Naval Command,
Control and Ocean
Surveillance Center RDT&E Division San Diego, CA
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Technical Report 1494
April 1992

1/f Noise in Indium Phosphide Transistors

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ADMINISTRATIVE INFORMATION

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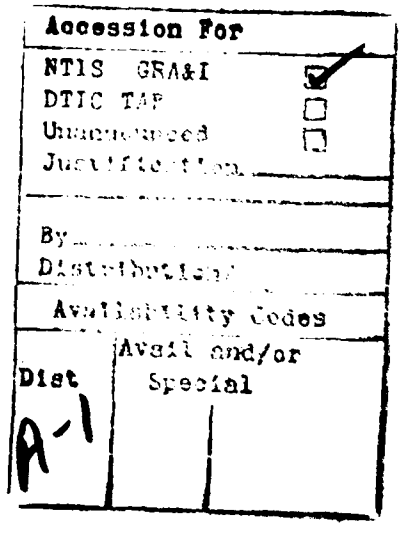
JT

EXECUTIVE SUMMARY

The sensitivity of an optoelectronic receiver is determined by its electrical noise. We found that integrated optical receivers made in the past decade are much noisier than hybrid receivers. When the accepted receiver model of Smith and Personick was examined for the cause of this discrepancy, we quickly discovered that the model was missing an important noise source. Is this source, 1/f noise, neglected by Smith and Personick?

With funding from the NRaD independent exploratory development (IED) program, this question was investigated during FY 91. The goal of the project, given the designation ZF04, was to examine indium-phosphide junction field-effect transistors for 1/f noise, first at frequencies below about 1 MHz, and next at frequencies between 1 MHz and 1 GHz. An auxiliary goal, to be carried out with additional funding from the Naval Research Laboratories, was to measure the optical sensitivity of a receiver circuit made from these same transistors and to correlate the optical sensitivity of this circuit with the electrical noise of the transistors. We found that our transistors and circuits do indeed have 1/f noise. The noise corners are within a factor of two of 50 MHz. Since our transistors are probably representative of the indium-phosphide technology as a whole, this means that indium-phosphide-based receivers operating below about 100 MHz will display extra 1/f noise. Circuits operating above about 1 GHz will still have the 1/f noise, but its contribution will be negligible.

Current circuits operate in the 1- to 10-GHz range and beyond. 1/f noise is most likely not missing noise source in these cases. The missing noise source at high frequency has not been found, and the discrepancy referred to above remains unexplained in that region.



CONTENTS

FIGURES

BACKGROUND

THE RELATIONSHIP OF ELECTRICAL NOISE TO OPTICAL RECEIVER SENSITIVITY

An optoelectronic receiver, figure 1, is a circuit that senses a weak optical signal, amplifies it, and converts it into an electrical signal. The arriving optical signal consists of bursts of photons, each burst representing a one, interspersed with periods of darkness, each such period representing a zero. The photodiode converts the photons, when present, to electrons that flow through the resistor, developing a voltage at the gate of the transistor. This gate voltage modulates a larger current flowing in the transistor leg of the circuit, resulting in a strong electrical signal at the output node of the circuit.

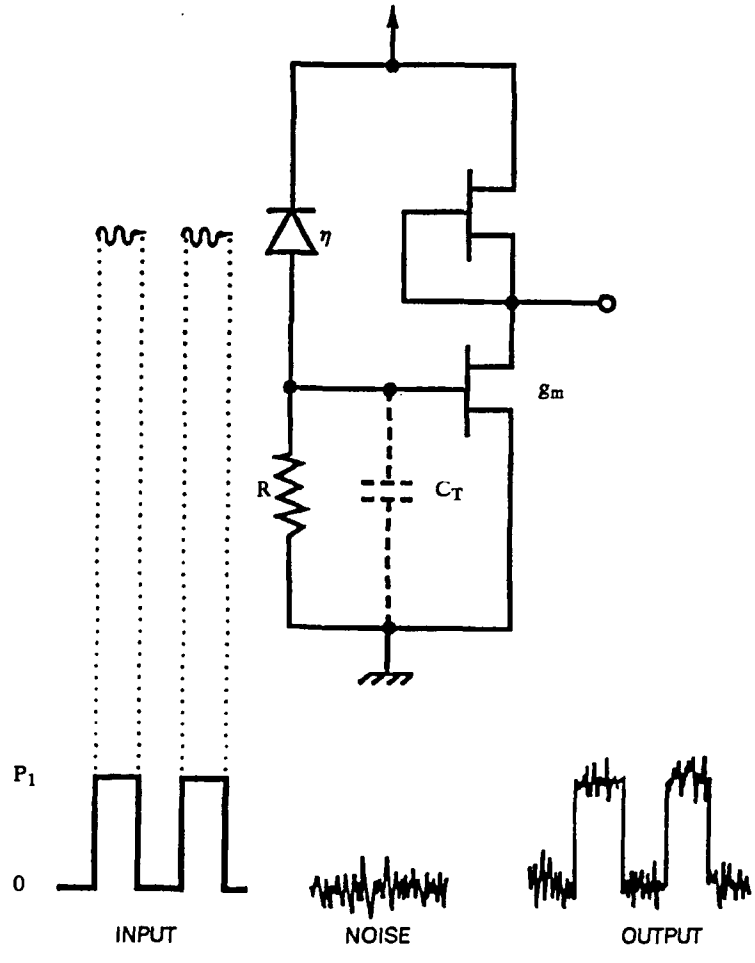


Figure 1. The essential components of an optical receiver.

As indicated schematically at the bottom of figure 1, electrical noise in the circuit will generally be present and will add to the relatively clean (but weak) optical signal producing a noisy electrical output. To restore the clean nature of the original digital signal, this first stage is followed by other circuits. A threshold level, typically halfway between the electrical zero and one levels, is established and used as a reference with which to compare samples of the signal. Any signal sample above the threshold counts as a one; any signal below counts as a zero. These data are then used to trigger a final circuit that will, for example, drive a laser, retransmitting the signal in optical form. The entire combination would then be an optical repeater.

With the idea of the threshold in mind, we can easily see how electrical noise can lead to an error in the retransmitted signal. For very weak optical signals at the input, the signal-to-noise ratio at the output will be small, and it will not be unusual for a noise spike on top of an electrical one to carry the voltage momentarily below the threshold, causing a zero if the timing should cause a sample to occur at the instant when the noise spike exists.

These ideas are based on an accepted model (Smith and Personick, 1980) that provides a mathematical relationship between electrical noise and optical sensitivity for an optical receiver circuit. The major features of this model are summarized in equations 1 to 4 of appendix A. Appendix A consists of a discussion of possible causes for the relatively poor sensitivity of monolithic receivers compared to hybrid receivers. One of the interesting features to arise from this comparison is the recognition that the monolithic receivers are noisier in actual fact than would be predicted by the accepted model. (This discrepancy is shown in figure 1 of appendix A by the separation between open and closed circles: the closed circle gives the actual sensitivity, the open circle gives the predicted sensitivity.) What is the extra noise? It might be the 1/f noise that is neglected in the model. This explained the discrepancy in the only case (Matsuda, et al., 1988) for which the electrical noise was investigated in addition to the optical sensitivity. Guided by this result we decided to examine the noise of our transistors to see whether 1/f noise might be present. We found that 1/f noise was present. Figure 2 gives a representative result for one of our own field-effect transistors (FETs) showing that 1/f noise with a noise corner frequency f_c of 50 MHz occurs. For the importance of this result, we offer the following formula:

$$\overline{i_c^2} = 16\pi^2 kTI_3 \left[\frac{\Gamma}{g_m}\right] [C_d + C_w + C_{gs}]^2 [1 + (3/2)(f_c/B)]B^3 \qquad (1)$$

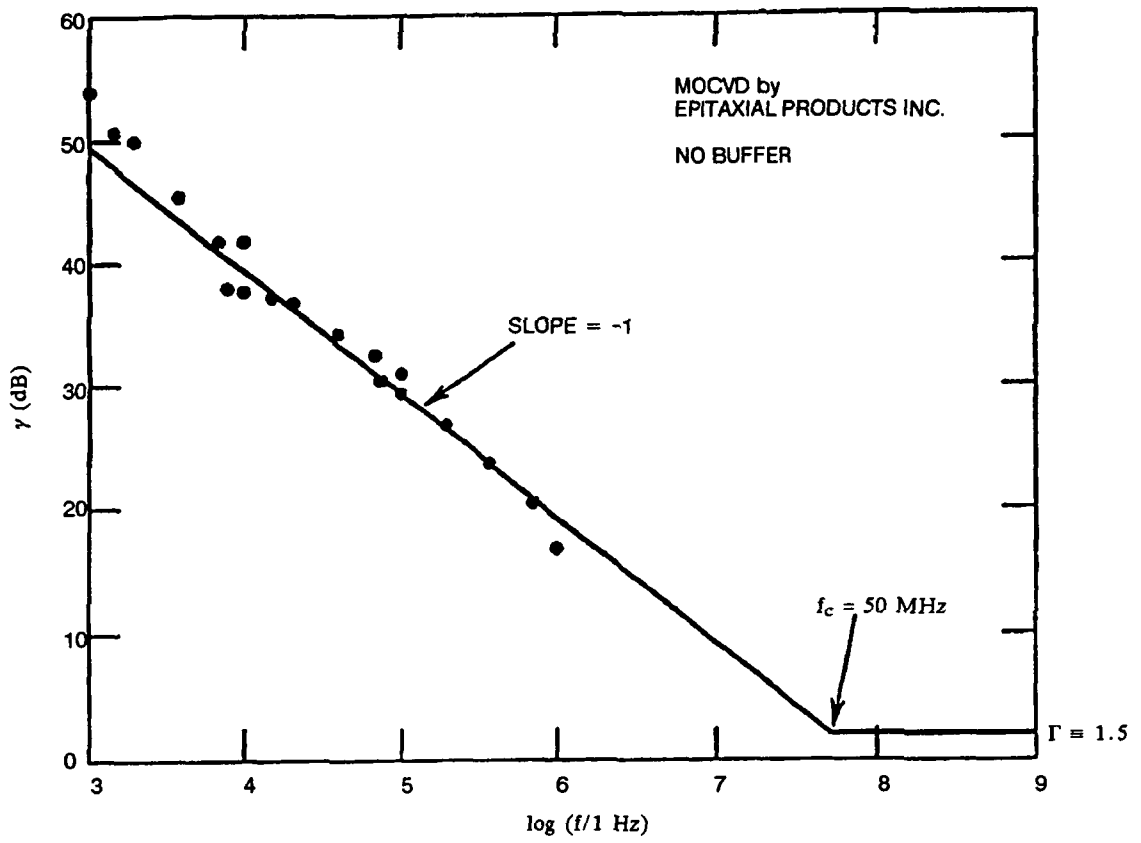


Figure 2. Noise spectrum of a transistor processed in our laboratories.

for the wide-band receiver noise arising from channel noise in the front end FET. The meaning of each symbol is given in part 3 of appendix A. Thus for a bit rate (the bit rate is equal to the reciprocal of the bit period) B of 100 MHz, the data of figure 2 imply an additional contribution of

$$\frac{3f_c}{2B} = \frac{3}{4} \tag{2}$$

or 75 percent to the mean-square FET noise where FET noise given by equation 1 dominates over the other two noise sources that are shot noise in the dark current and Johnson noise in the current sensing resistor. Since the optical sensitivity is proportional to the square root of all mean-square noises added in quadrature (equation 4 of appendix A), this equation implies a sensitivity reduction by a factor of

$$\sqrt{\frac{3}{4}} = 1.323 \approx 1.2 \text{ dB} \tag{3}$$

due to the presence of 1/f noise. As the bit rate increases, 1/f noise plays a diminishing role; for example, 1/f noise with noise corners on the order of 100 MHz can be confidently neglected when operating circuits at bit rates of a GHz or more.

THE MEASUREMENT METHOD IN BRIEF

Figure 3 shows the low-frequency equivalent circuit representing a junction field effect transistor (Gray and Meyer, 1984). The incremental mean square noise current $d < i_n^2 >$ per incremental bandwidth df is (Gray and Meyer, 1984)

$$\frac{d < i_n^2 >}{df} = (4kTg_m)\left(\Gamma + \frac{f_c}{f}\right) \tag{4}$$

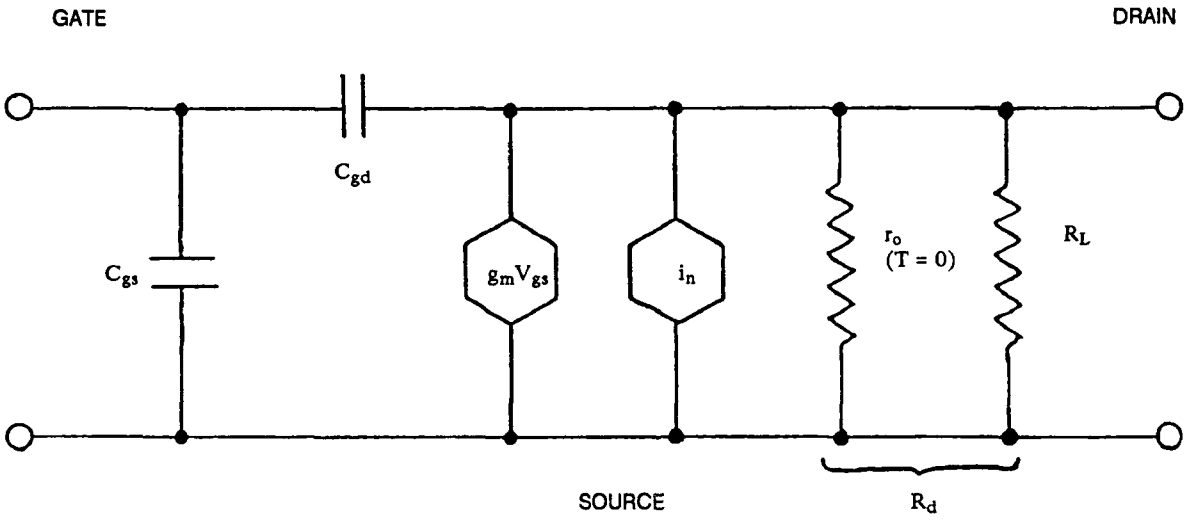


Figure 3. Low-frequency small-signal equivalent circuit for a junction field-effect transistor. The output resistance r_o is a dynamic quantity that contributes no noise.

where $f_c \equiv (KI_D{}^a)/(4kTg_m)$ is a frequency-independent parameter called the noise-corner frequency. Γ is a numerical constant on the order of unity that characterizes the channel noise of the transistor. The channel noise is independent of bandwidth, or "white." For silicon transistors, Γ has the value of two thirds. For gallium-arsenide transistors (and probably indium-phosphide transistors) Γ has the value of three halves. We can

see from equation 4 that in addition to channel noise, 1/f noise also occurs with a "pink" spectrum that rises as the frequency falls like 1/f. Defining

$$\gamma = \Gamma + \frac{f_c}{f} \tag{5}$$

we have

$$\frac{d < i_n^2 >}{df} = 4kTg_m\gamma. \tag{6}$$

Our goal is to devise a method to measure γ. In figure 4, a plot of the logarithm of γ versus the logarithm of frequency will have a slope of −1 and will intersect a straight line whose value is log Γ at a frequency f_c, the so-called "noise-corner frequency."

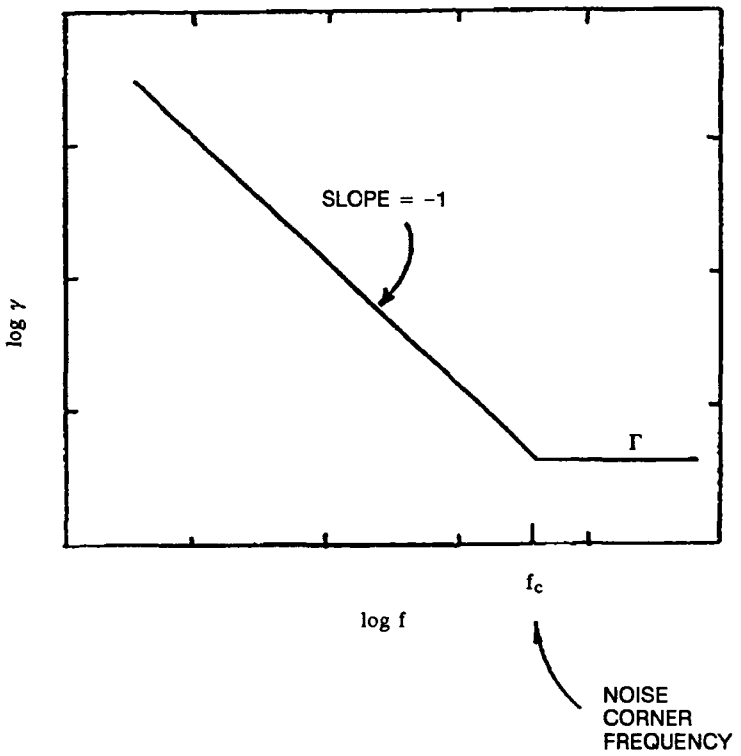


Figure 4. Dependence of the transistor channel and 1/f noise factor, γ, on frequency.

The method for measuring γ is as follows:

1. Apply the transistor under investigation to the input of a preamplifier with an available power gain of G and a noise figure of F. Let the low-frequency transconductance of the transistor be g_m. Apply a bias to the drain of the transistor through a load resistor R_L. Measure the output noise power of the preamplifier, $N_o(f)$, with the spectrum analyzer. Figure 5 shows the set-up.

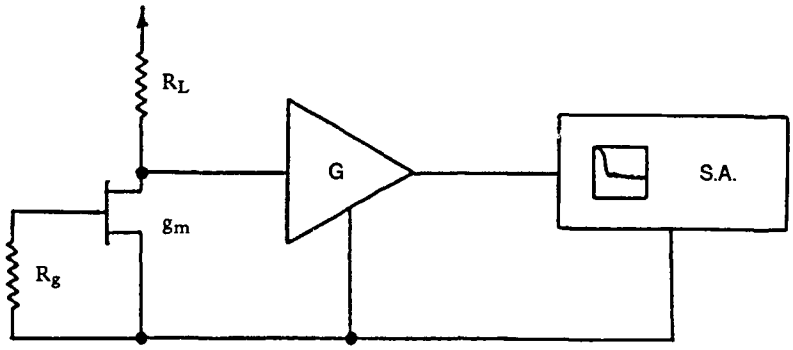


Figure 5. Experimental set-up for measuring the transistor and preamplifier noise power.

2. Replace the transistor with the load resistor R_L. Measure the new output-noise power of the preamplifier, $N_o'(f)$, with the spectrum analyzer. Figure 6 shows this set-up.

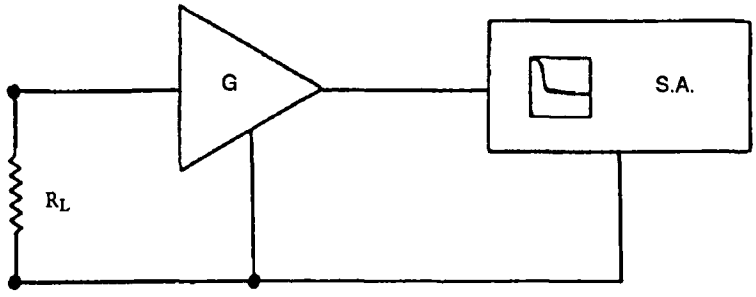


Figure 6. Experimental set-up for measuring system available power gain.

3. Form the ratio ρ(f) of the two noise powers:

$$\rho(f) = \frac{N_o(f)}{N_o'(f)} \tag{7}$$

4. Appendix B shows it is approximately true that

$$\gamma = \frac{F\rho(f)}{g_m R_d}. \tag{8}$$

Here R_d is the parallel combination of R_L and r_o, the noise-free output resistance of the transistor. Since $R_L \approx 100\ \Omega$ and $r_o \approx 1\ \text{k}\Omega$, $R_d \approx R_L$. The value of F is not a strong function of frequency within any given decade and can be taken from the preamplifier manual. (A safer procedure would probably be to measure F directly.)

5. Plot log $[F\rho(f)]/[g_m R_d]$ versus log (f/1 Hz). The slope should be -1 for true 1/f behavior. The intercept of these data with log(Γ) = log (3/2) will give the noise corner f_c for this particular device.

This method will in principle work at any frequency for which the equipment is designed and for which the equivalent circuit of figure 3 remains valid. In actual practice, the method breaks down high in the MHz range because preamplifiers designed for the GHz-frequency range do not operate unless they are terminated at both ends with a 50 Ω impedance. This impedance causes no problem at the output since spectrum analyzers are designed with 50 Ω input impedances. However, our FETs have output impedances of $r_o \approx 1\ \text{k}\Omega$, a mismatch to the input of the high-frequency preamplifier that causes the high-frequency preamplifier to oscillate unless a matching network is used.

DEVICE STRUCTURE

Figure 7 is a cross section of the device used in this discussion. The channel was an epitaxial layer of n-type InP(Si) grown to a thickness of 250 ±50 nm by OMVPE on a substrate of semi-insulating InP(Fe). (Material supplied by Epitaxial Products International, Ltd., Cypress Drive, St. Mellons, Cardiff CF3 OEG UK.) The electron concentration in the channel layer was $(1.5 \pm 0.5) \times 10^{17}\ \text{cm}^{-3}$. This device was labeled "Device B" of process run "MODFET-34" carried out during the months of November and December 1990. Individual devices were isolated by mesa etching. Source and drain ohmic contacts consisted of Au-Ge metal deposited by evaporation, defined by lift-off, and annealed at 375°C for 10 minutes. The gate region was recessed until a source-drain current of 35 mA was obtained and gate metal (Chang, et al., 1982) was evaporated into the recess. The gate metal consisted of the following layers: 2.5 nm Au/5 nm Zn/2.5 nm Au/5 nm Zn/5 nm Au. The gate length and width were 1 μm and 400 μm, respectively. The device was annealed at 375°C in argon for 1 minute to simultaneously create and make contact to a p+ region in the n-type channel. Figure 8 shows a plan view of the T-gate transistor structure.

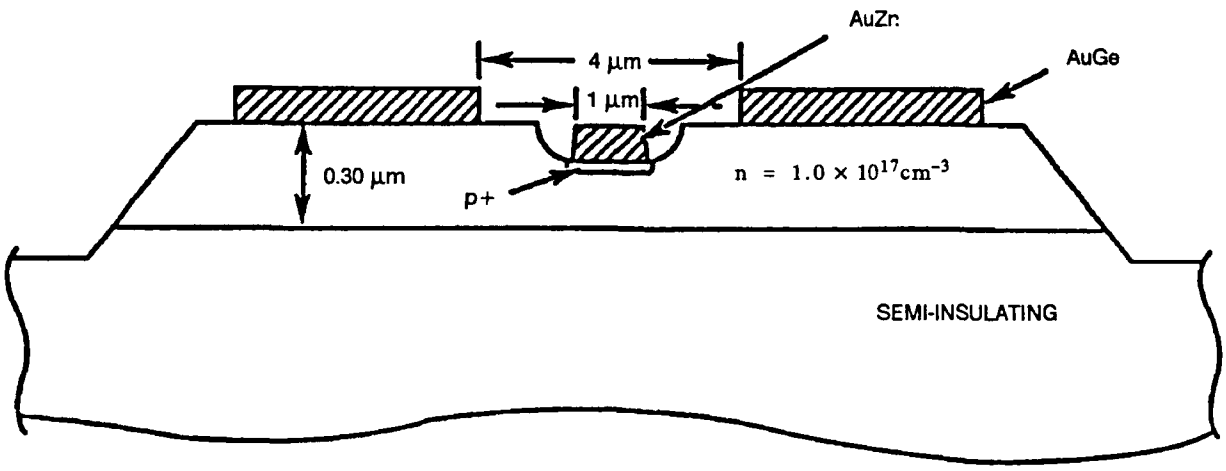


Figure 7. Cross section of junction field-effect transistor used in this study.

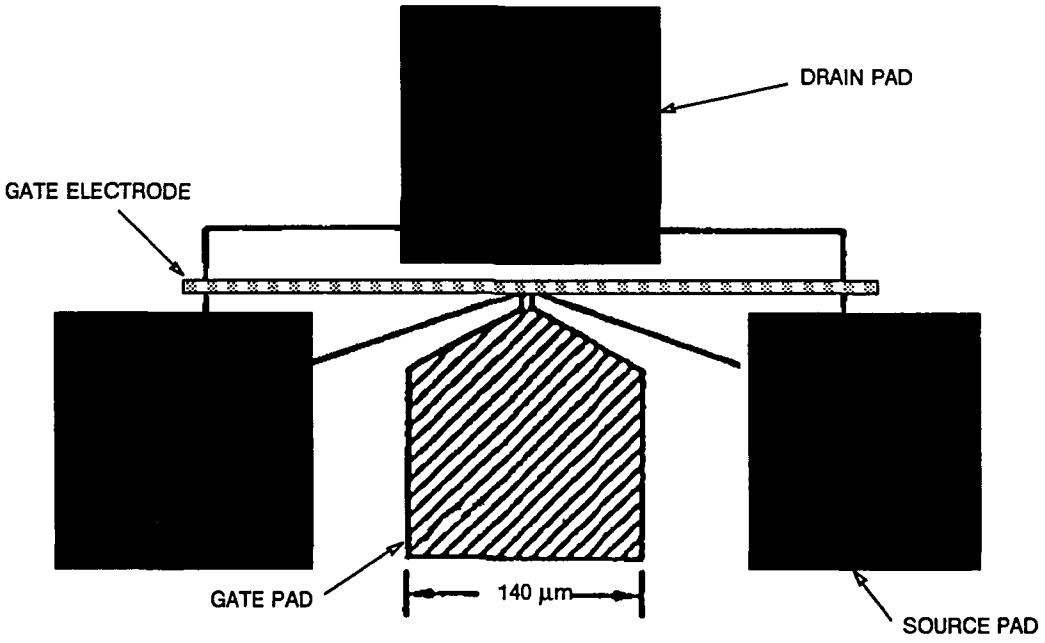


Figure 8. Plan view of T-gate transistor structure.

The device was cleaved from the wafer, epoxied to a copper carrier with the source grounded through a drop of epoxy, and the gate and drain were wire bonded to 50 Ω transmission lines terminated in SMA connectors.

The transconductance g_m was measured with a curve tracer on December 4, 1990. The characteristic is shown in figure 9. At a drain-to-source voltage of 1.5 V and a

gate-to-source voltage of 0 V, the transconductance is 32 mS. The output conductance at a gate-to-source voltage of −1.5 V (the bottom trace in the photograph) is about 2.5 mA/5 V ≈ 0.5 mS. The reciprocal of this conductance is the output resistance r_o, about 2 kΩ.

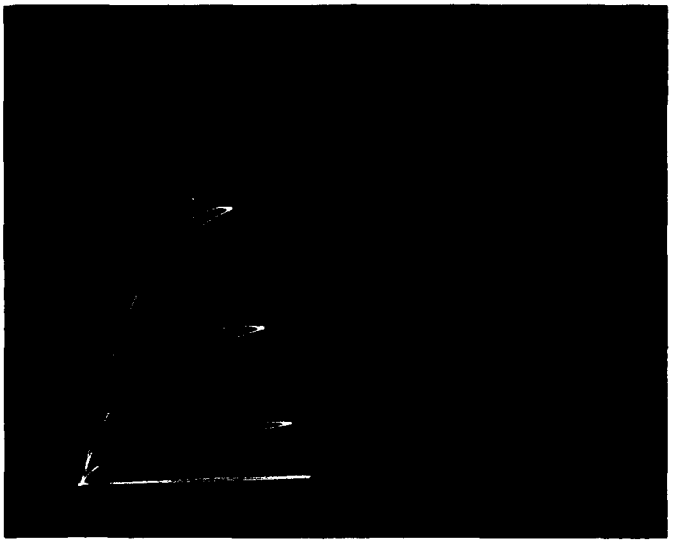


Figure 9. I(V) characteristics of device B of process run MODFET-34.

THE MEASUREMENT METHOD IN DETAIL

On March 28, 1991, the noise of Device B was measured with a Hewlett Packard model 8566B spectrum analyzer using the method previously outlined. The set-up is given in figure 5. The preamplifier was a PAR Model 113 with a voltage gain of 1000, AC coupled, with a bandpass of 1 to 300 kHz. The FET power supply was a set of batteries. The load resistor was 100 Ω. The gate resistor was 50 Ω. These values give $g_m R_d \approx g_m R_L \approx 3.2 \approx 5$ dB. The noise figure of the preamplifier, taken from the preamplifier manual, was 12 dB and approximately constant for this frequency range.

Figure 10 shows the supply did not contribute any noise. Figure 10 actually consists of two separate traces from the spectrum analyzer that overlap so closely they cannot be distinguished. The first trace was made with the set-up of figure 5 (FET, load resistor, and supply in front of preamplifier) with a supply voltage of 0 V. The second trace was made with the set-up of figure 6 (load resistor in front of preamplifier). The

overlap of these traces allowed a simplification: set up as in figure 5; turn the supply on to measure N_o, the numerator of ρ; turn the supply off to measure N_o', the denominator of ρ. Figure 11 shows the output of the spectrum analyzer when this simplification is adopted. The top trace is with the supply set to 4.5 V resulting in a drain voltage of 1.43 V. This is a measure of N_o. The bottom curve is with the supply set to 0 V. This top trace is a measure of N_o'. Since this spectrum analyzer display gives the logarithm of noise power along the ordinate, the difference between these two traces is $\rho = N_o/N_o'$ on a log scale. For example, at the far right hand side of figure 11, at 1 MHz, this difference (hence ρ itself in dB) is 10 dB since each vertical division is 10 dB in this figure.

We have the following data for this device at 1 MHz:

$$\rho = 10 \text{ dB},$$

$$F = 12 \text{ dB},$$

$$g_m R_d = 5 \text{ dB},$$

$$\text{and } \gamma = F\rho/g_m R_d = 17 \text{ dB}.$$

Figure 12 is a plot of γ versus f/(1 Hz) on a log-log scale. Following our 1 MHz example through to its conclusion, please note that the final datum at 1 MHz in this figure is correctly located at 17 dB. The other data come from the same procedure repeated at different frequencies. The data can be fit by a straight line with a slope of −1 which intersects $\log(\Gamma) = \log(1.5)$ at a noise-corner frequency of 50 MHz.

RESULTS

The structure of figure 7 with commercial epitaxial material gave the results of figure 12: 1/f noise was observed with a noise corner of 50 MHz. We commonly thought that 1/f noise arises from traps in the active channel layer (Hughes, et al., 1987), although many other sources have also been cited. However, traps are the primary suspect. There are two ways to manipulate traps: (1) try different epitaxial material and hope that it will be trap free, and (2) grow a thick buffer layer and hope that traps in the substrate will not be propagated into the active material (that is assumed trap free).

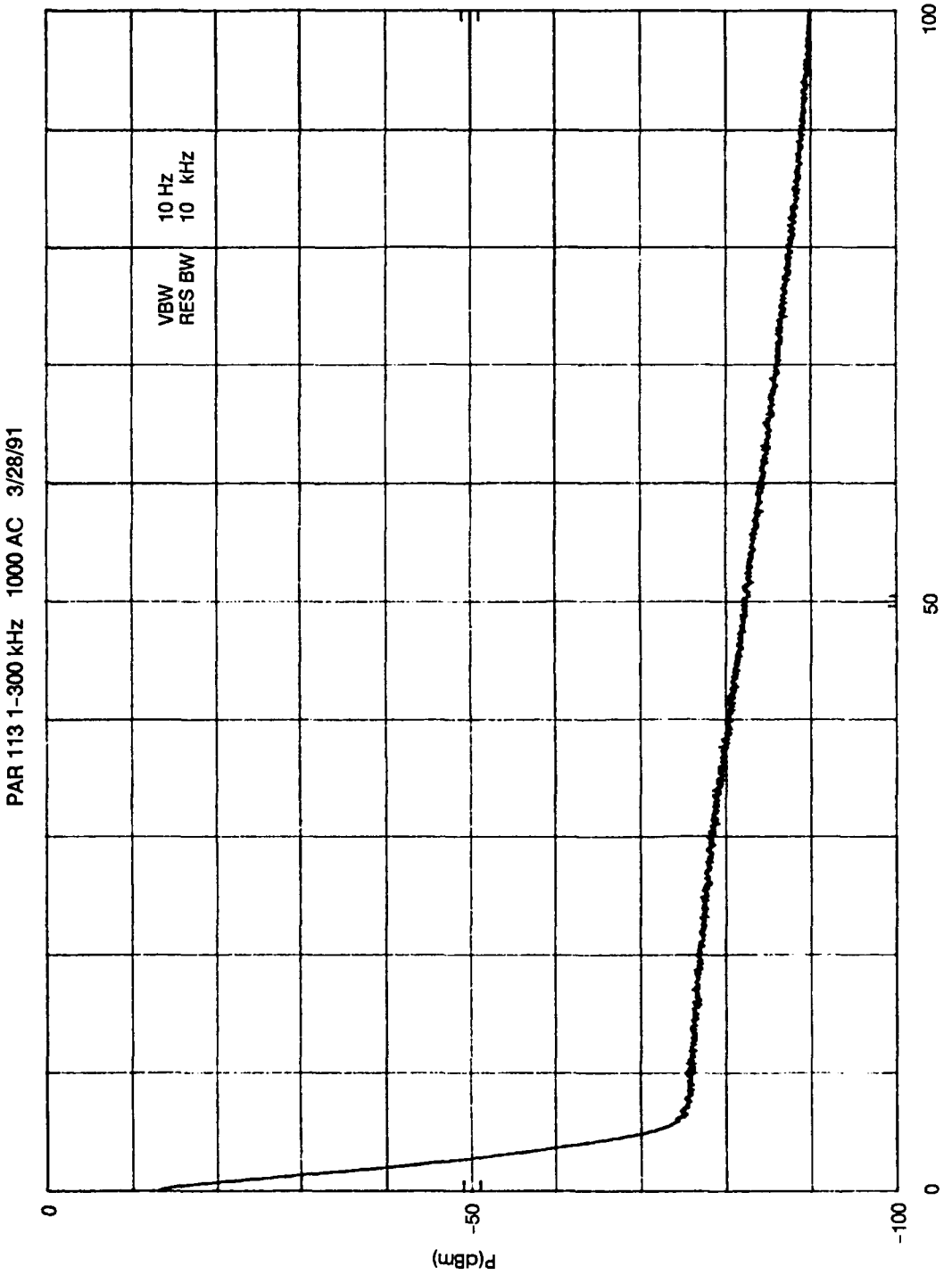


Figure 10. Spectrum analyzer plot. Trace 1: 100 Ω at preamplifier input. Trace 2: FET device B with bias set to 0 V at preamplifier input. (The traces completely overlap.)

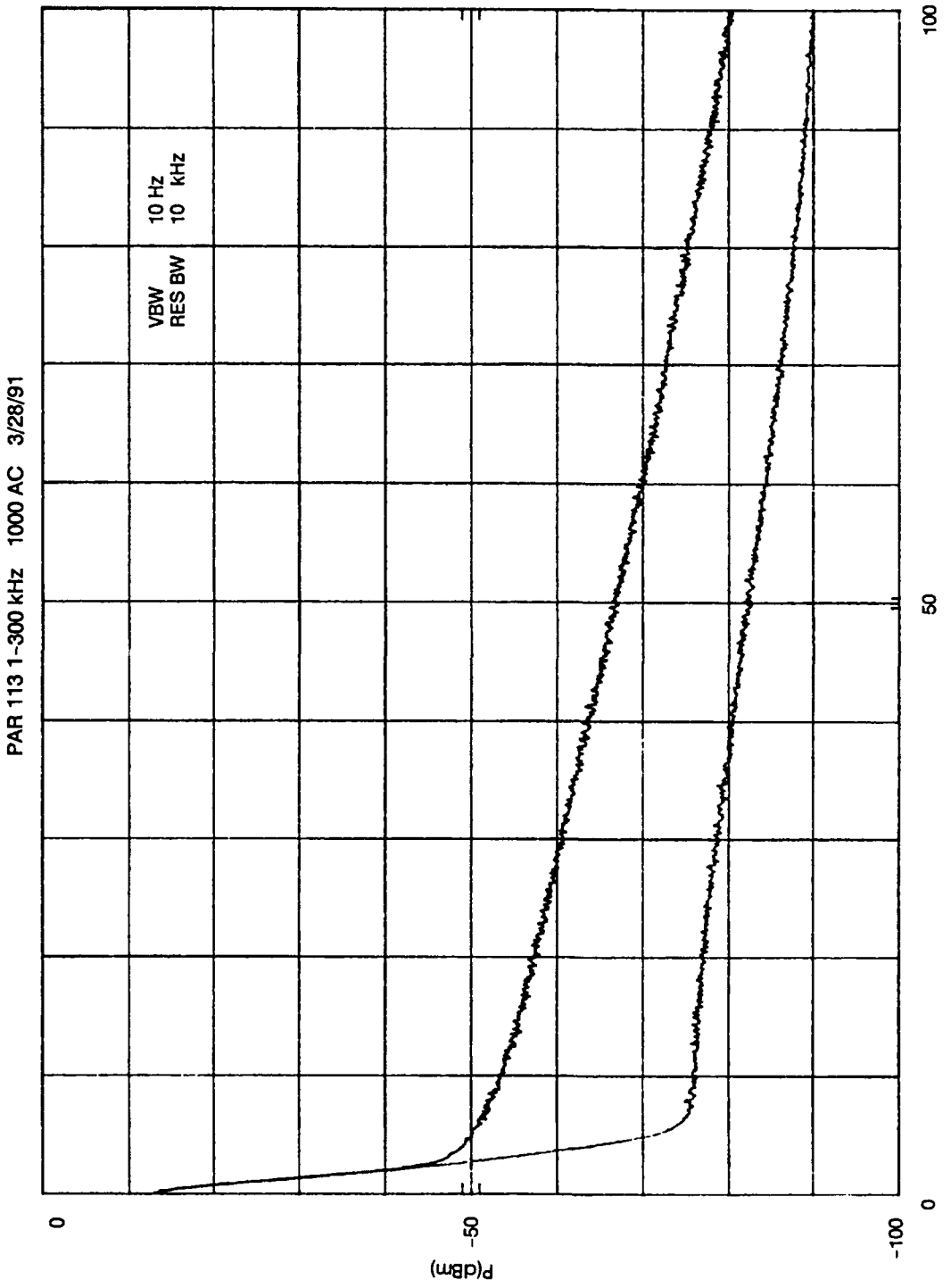


Figure 11. Spectrum analyzer plots. Lower trace: Device B with 0 V bias. Upper trace: Device B with 1.43 V drain bias.

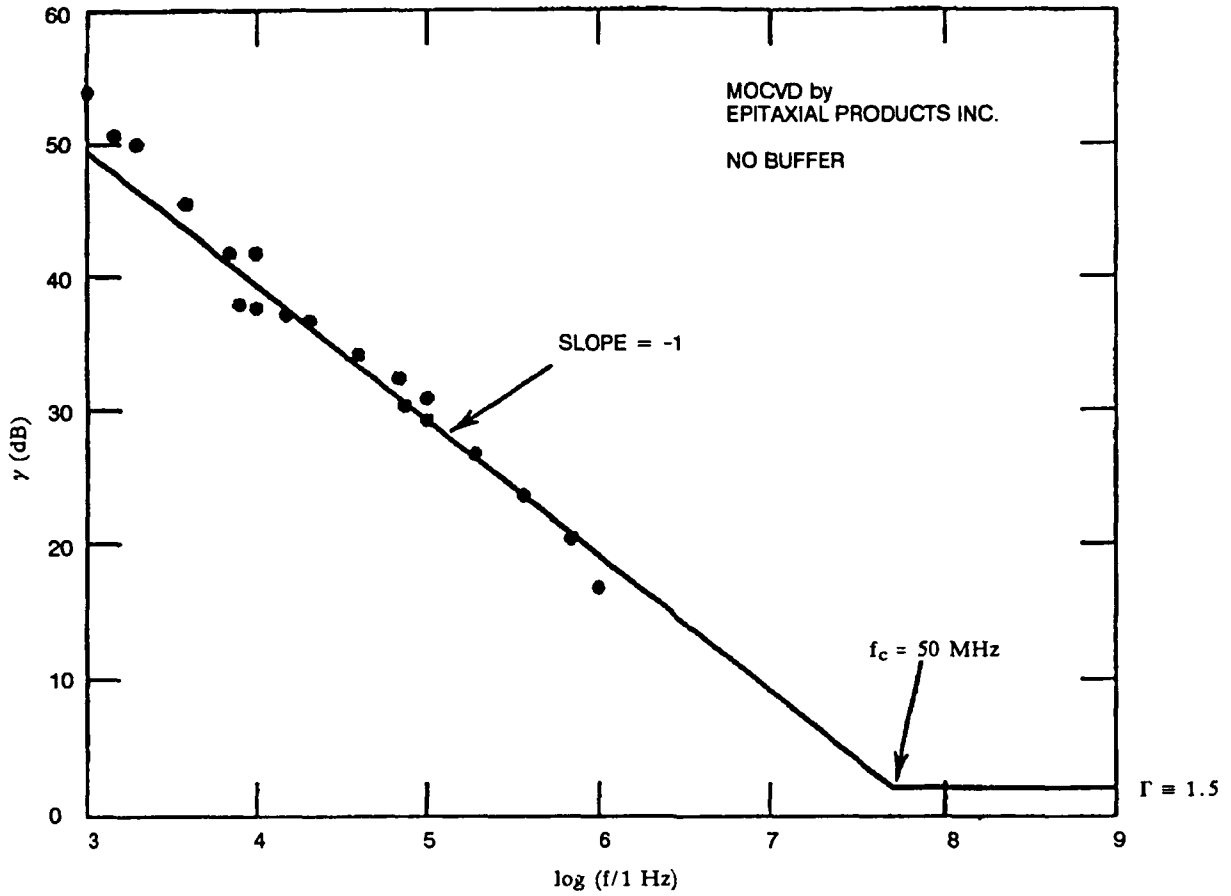


Figure 12. Noise spectrum of device B. The noise corner frequency is 50 MHz.

Both of these methods were tried: (1) The structure of figure 7 was duplicated by carrying out OMVPE growth in our own laboratories. The method of the previous section was used to measure the noise spectrum of this new transistor material. Figure 13 shows the results. The noise corner has not been significantly changed. (2) The structure of figure 14 was grown with the results shown in figure 15. The slight reduction in noise-corner frequency should not be regarded as significant given the spread in the data.

We see that neither different epitaxial material nor the presence of a buffer layer has caused a significant reduction in the amount in 1/f noise seen in indium-phosphide junction field-effect transistors as they are made in our laboratories.

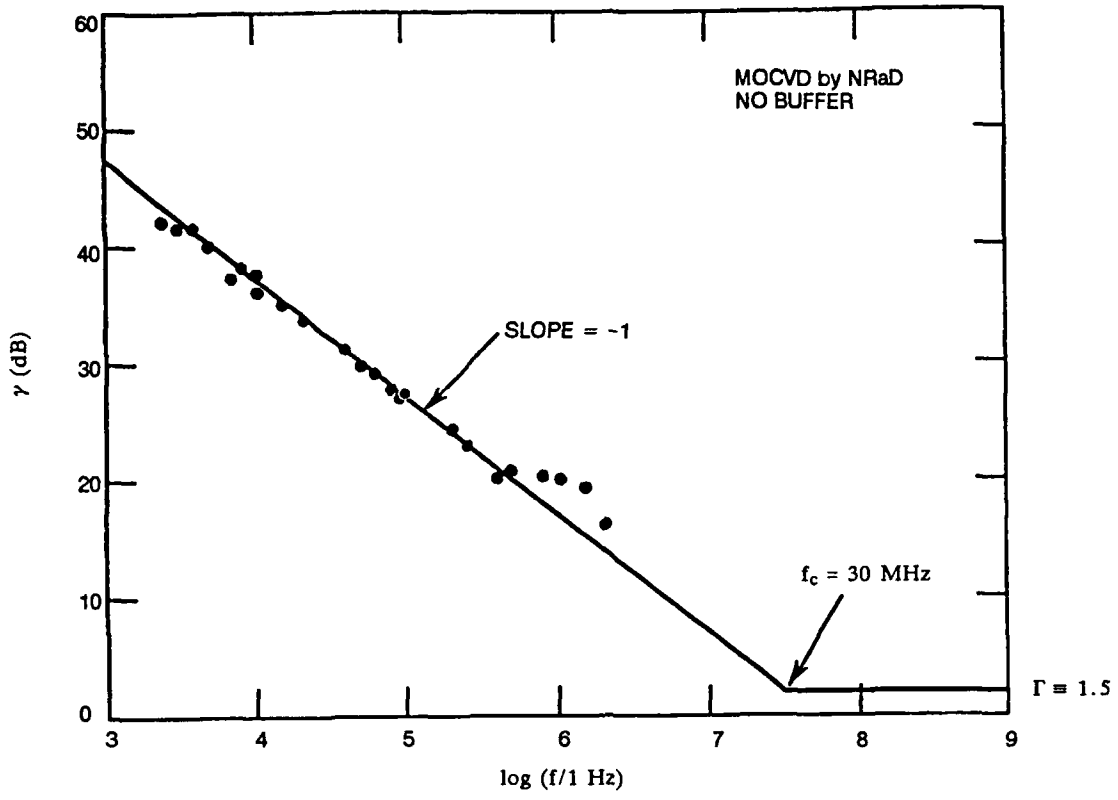


Figure 13. Noise spectrum of a transistor with NRaD epitaxial material. The structure is given in figure 7.

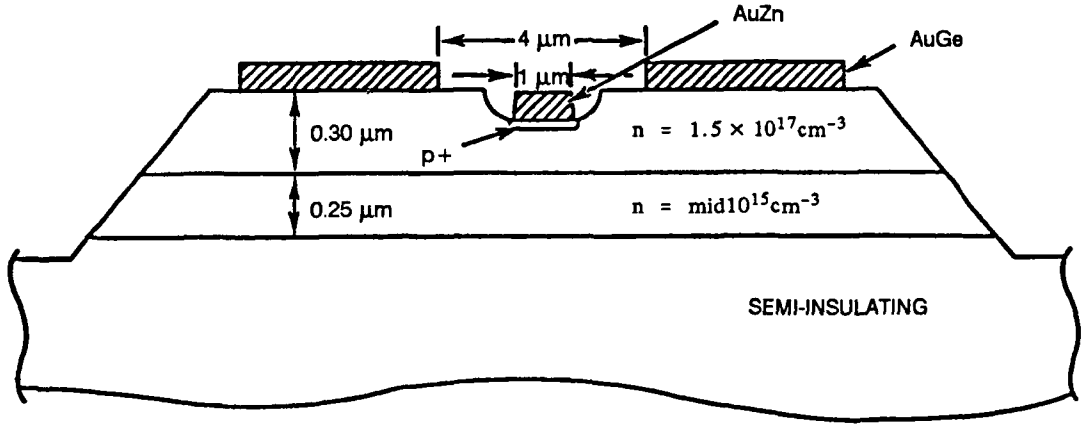


Figure 14. Structure of transistor grown in NRaD laboratories with a 0.25-micron buffer layer.

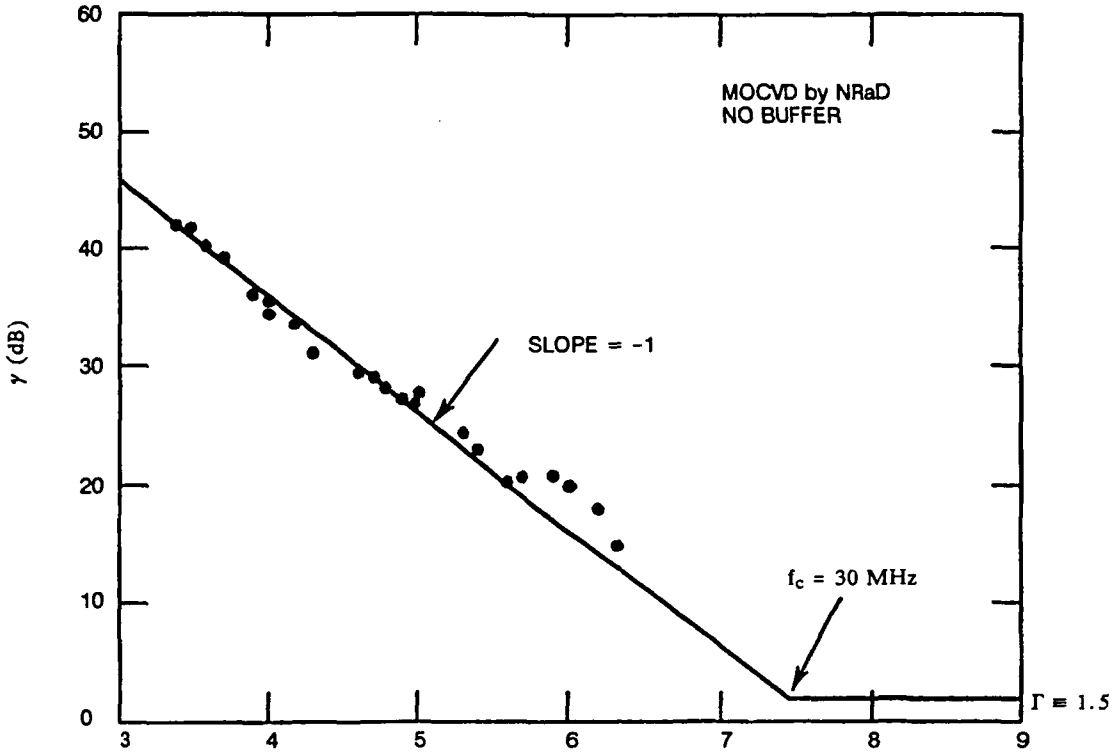


Figure 15. Noise-power spectrum of transistor with a buffer layer grown in NRaD laboratories. The layer structure of the transistor is given in figure 14.

CONCLUSION

1/f noise does indeed exist in indium-phosphide junction field-effect transistors as they are made in our laboratories. Noise corners are within a factor of two of 50 MHz, independent of the source of epitaxial material (at least for the two sources tested), and also independent of the presence of buffer layers whose thickness is a fraction of a micron.

1/f noise degrades the optical sensitivity of circuits operating with bit rates into the 100-MHz range, but is negligible for higher bit rates. Since current circuits are operating at bit rates of 10 GHz and more, 1/f noise can confidently be neglected in these high-speed applications.

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APPENDIX A

"Sensitivity of optoelectronic receivers"

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for Advanced Electronic and Optical Devices

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Sensitivity of optoelectronic receivers

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ABSTRACT

The formula used to predict wide-band noise of optoelectronic receivers has been modified to account for parasitic resistances in the transistor connected to the photodiode. The new formula leaves the total noise unchanged after proper steps have been taken to adjust the transistor gate width for minimum noise. The discrepancy between measured and predicted noise of 1.65 μm monolithic InP receivers thus remains largely unexplained.

1. INTRODUCTION

Optoelectronic receivers sensitive to 1.65 μm radiation have been made by: (1) monolithic integration[1-7] of an InGaAs photodiode with InP or InGaAs FETs on a single InP substrate and (2) hybrid combination[8-10] of an InGaAs photodiode with GaAs MESFETs. Because monolithic circuits can, in theory, have smaller parasitic capacitances than hybrid circuits, they are usually regarded as capable of higher speed and higher sensitivity. However, the monolithic circuits built to date have been consistently less sensitive than hybrid circuits. Since low optical sensitivity is a direct reflection of high electrical noise, this means that monolithic receivers built to date have been noisier than hybrid receivers. In this paper we are interested in examining possible causes for the high noise of the monolithic circuits.

2. RECEIVER NOISE

The measured sensitivities of some monolithic and hybrid receivers are shown in Fig. 1 by the solid symbols. The monolithic receivers are roughly 10 dbm, or an order of magnitude, less sensitive than the hybrid receivers. To examine the source of this difference, it may be useful to calculate the sensitivity expected of the

412 / SPIE Vol. 1144 Indium Phosphide and Related Materials for Advanced Electronic and Optical Devices (1989)

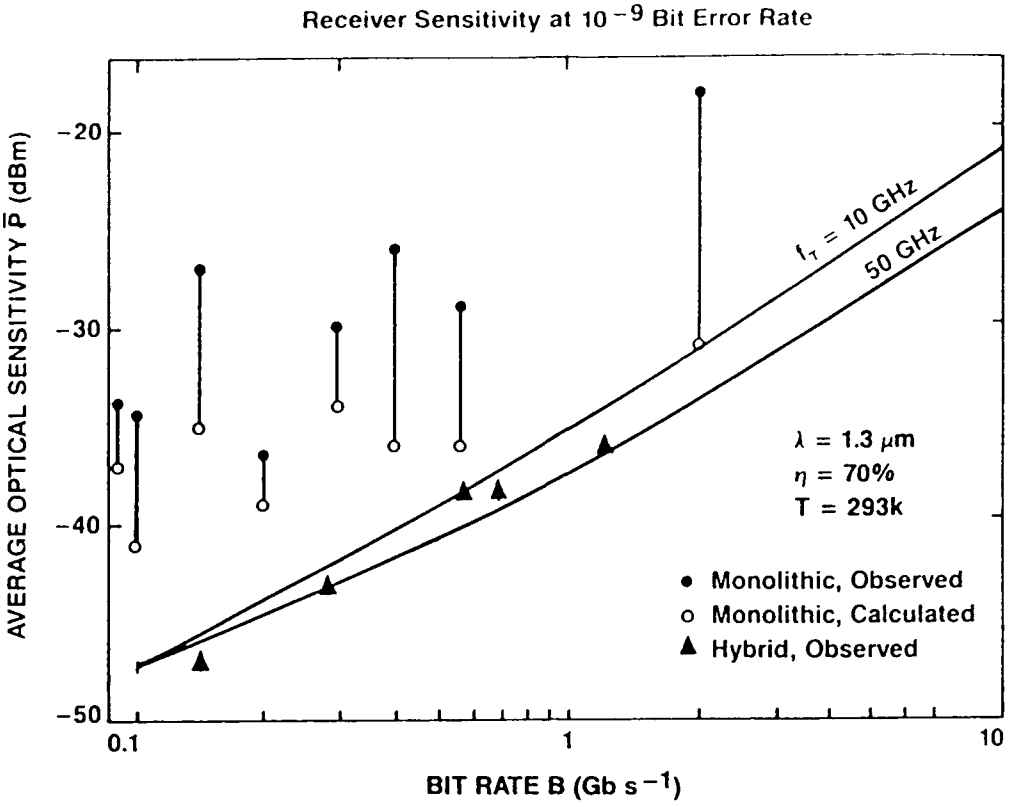

Figure 1. The observed sensitivity of some monolithic (●) and hybrid (▲) receivers reported in the literature. The open symbols (○) represent the sensitivity predicted for each monolithic receiver from its critical circuit elements. The solid lines represent the minimum sensitivity which could be achieved with FETs of the indicated f_T.

monolithic circuits. This has been done following the model of Smith and Personick[11], summarized in the next section. The critical circuit elements for each monolithic circuit, listed in Table 1, have been used with this model to predict each sensitivity shown in Fig. 1 as an open circle. Two features are immediately evident: (1) the predicted sensitivities do not match the hybrid results and (2) the measured sensitivities fall short of the predicted results.

Is it possible that some significant noise source has been neglected in the standard model? If so, it would improve the agreement between theory and experiment, reduce the second discrepancy, and point the way toward increasing the monolithic

Ref.	B (Gb s^{-1})	I_d (nA)	R (kohm)	C_T (pF)	g_m (mS)	f_T (GHz)
1	0.1	3	106	2.9	8.8	3.6
2	0.14	30	1	2.4	7	0.9
3	0.2	10	30	1.5	10	9
4	0.295	25	1.5	1.5	10	2.3
4	0.09	25	1.5	1.5	10	2.3
5	0.4	5	10	1	6	6.4
6	0.56	2000	100	0.7	8.8	13
7	2	1000	5	0.2	4	6.4

Ref.	$\overline{i_c^2}$ (A^2)	$\overline{i_j^2}$ (A^2)	$\overline{i_s^2}$ (A^2)	$\overline{P}_{calc}$ (dBm)	$\overline{P}_{obs}$ (dBm)	$\overline{P}_{min}$ (dBm)
1	4.8×10^{-20}	8.3×10^{-18}	7.5×10^{-17}	−41	−34.5	−47
2	6.7×10^{-19}	1.2×10^{-15}	1.8×10^{-15}	−35	−27.1	−46
3	3.2×10^{-19}	5.5×10^{-17}	1.4×10^{-16}	−39	−36.4	−44.5
4	1.2×10^{-18}	1.6×10^{-15}	4.5×10^{-16}	−34	−30	−43
4	3.6×10^{-19}	5.0×10^{-16}	1.3×10^{-17}	−37	−34	−47.5
5	3.2×10^{-19}	3.3×10^{-16}	8.4×10^{-16}	−36	−26	−41.5
6	1.8×10^{-16}	4.6×10^{-17}	7.7×10^{-16}	−36	−29	−40
7	3.2×10^{-16}	3.3×10^{-15}	6.3×10^{-15}	−31	−18.5	−33.5

Table I. Critical circuit elements and their noise contribution to seven monolithic receivers. The noise currents have been converted to a predicted sensitivity ($\overline{P}_{calc}$) by assuming a wavelength of 1.3 microns, a quantum efficiency of 70%, and a bit error rate of 10^{-9}. The sensitivity actually observed ($\overline{P}_{obs}$) has been adjusted to these values wherever necessary. The minimum achievable sensitivity ($\overline{P}_{min}$) for 50 GHz FETs is given in the last column.

performance. Toward this end we will now summarize the Smith and Personick model, suggest a modification and examine the modified result.

3. THE STANDARD NOISE MODEL

According to a well known treatment[11] of receiver sensitivity, there are three major contributions to electro-optic receiver noise: (1) shot noise in the dark current, (2) Johnson noise in the current sensing resistor and (3) channel noise in the front end FET. In this model they are given, respectively, by the following expressions.

$$\overline{i_s^2} = 2qI_dI_2B \tag{1}$$

$$\overline{i_j^2} = \frac{4kT}{R} I_2B \tag{2}$$

$$\overline{i_c^2} = 16\pi^2kTI_3 \frac{\Gamma}{g_r} (C_d + C_w + C_{gs})^2 B^3 \tag{3}$$

where q is the electronic charge, I_d is the leakage current in the dark of the photodiode and front end FET, B is the bit rate, k is Boltzman's constant, T is the absolute temperature, and R is the amplifier transimpedance. Also, Γ is the drain noise coefficient (approximately 1.5), g_r is the FET transconductance, C_d is the capacitance of the diode, C_w is the capacitance of the wiring connecting the diode to the first FET, and C_{gs} is the gate to source capacitance of the FET. Finally, I_2 (typically 0.5) and I_3 (typically 0.08) are the Personick integrals relating the input and output pulse shapes.

These noise currents are added in quadrature and related to the average minimum detectable optical signal by

$$\bar{P} = \frac{Qhc}{\eta\lambda q}(\overline{i_s^2} + \overline{i_j^2} + \overline{i_c^2})^{1/2} \tag{4}$$

Here η is the diode external quantum efficiency, Q is equal to six for a bit error rate of 10^{-9} and λ is the wavelength of the incident optical radiation.

Taking T = 293 K, λ = 1.3 μm and η = 70% we have

$$\overline{i_s^2} = (1.602 \times 10^{-19})\ I_d\ B\ \ A^2 \tag{5}$$

$$\overline{i_j^2} = (8.28 \times 10^{-15})\ \frac{B}{R}\ \ A^2 \tag{6}$$

$$\overline{i_c^2} = (7.85 \times 10^{-14})\ \frac{C_T^2}{g_m}\ B^3\ A^2 \tag{7}$$

$$\frac{Qhc}{\eta\lambda q} = 8169\ \text{mW}\ A^{-1} \tag{8}$$

where $C_T = C_d + C_w + C_{gs}$. These expressions will be numerically correct if I_d is expressed in nA, B in Gbit s^{-1}, R in kohm, C_T in pF, and g_m in mS.

The least noise is obtained by keeping the dark current low, the sensing resistance as high as the bandwidth will allow, the total capacitance of the input node low, and the transconductance high for the first FET. At high speeds the channel noise will become progressively more dominant due to its cubic bit rate dependence.

4. THE MODIFIED NOISE MODEL

The FET imagined in the standard model just described is the ideal, or intrinsic, FET with no parasitic resistances. On the other hand, Fukui[12] has shown that the minimum noise figure of an actual FET is, to a good approximation, entirely due to the parasitic resistances R_g and R_s, where R_g is the resistance of the gate metal and R_s is the resistance of the undepleted channel between source and gate. These resistances are shown in the noise equivalent circuit of Fig. 2. The physical location of each element within the actual device is given in Fig. 3. We have extended the standard model to include these resistances. The derivation is outlined in the Appendix. The shot and Johnson noises, of course, remain unchanged, but the channel noise becomes

$$\overline{i_c^2} = 16\pi^2 kTI_3\ \frac{\Gamma}{g_m}\ (1 + \gamma)\ \{C_d + C_w + \frac{C_{gs}}{1 + \gamma}\}^2\ B^3 \tag{9}$$

where $\gamma = g_m\ (R_s + R_g)/\Gamma$.

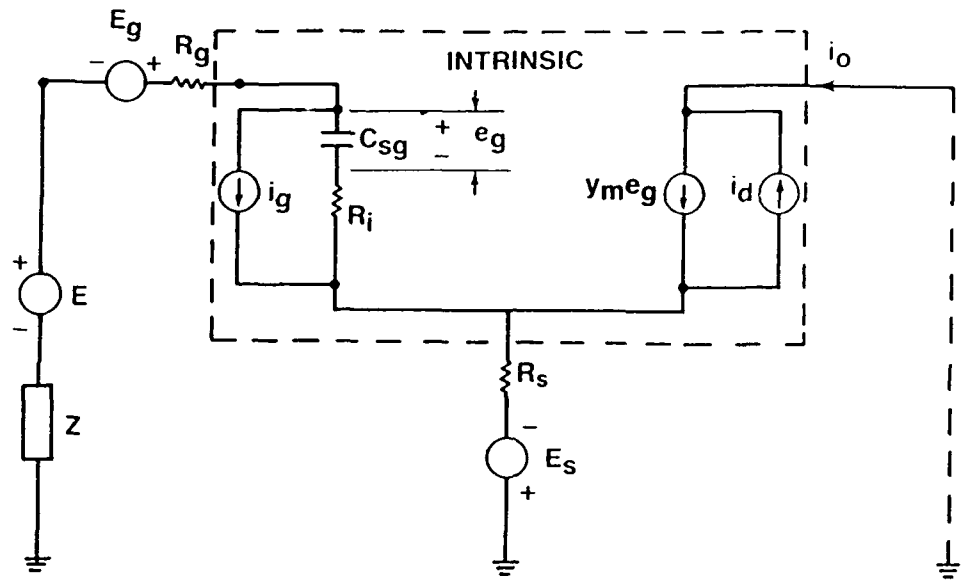

Figure 2. The noise equivalent circuit of the extrinsic FET used in the analysis of Pucel, Haus, and Statz. The intrinsic FET is included within the dashed box.

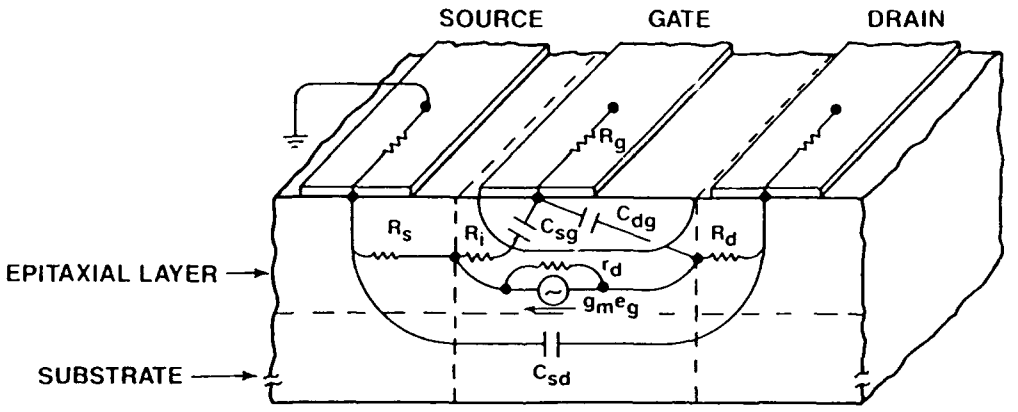

Figure 3. A cross-sectional view of the extrinsic FET showing the physical origin of the circuit elements represented in figure 2. After Pucel, Haus, and Statz.

This formula reduces to the one given in the standard model for $\gamma = 0$, the ideal case.

Ironically, this new equation changes the noise situation in only a subtle way. This comes about because the factor

$$\frac{\Gamma}{g_m}(1 + \gamma) = R_s + R_g + \frac{\Gamma}{g_m} \tag{10}$$

will in general be a function of gate width. For example, in a given technology the transconductance per unit gate width will be pushed to an upper limit and once that limit is reached the desired transconductance will be attained by scaling the width. Similarly, C_{gs}/W, R_g/W, R_sW, and $f_T = g_m/(2\pi C_{gs})$ will be approximately constant in any given FET technology. Obviously, the value of W should be adjusted to minimize the channel noise. Simple algebraic examination shows that the minimum mean square noise current will be

$$\overline{i_c^2}\Big|_{min} = 32\pi kT\Gamma I_3 \frac{C_d + C_w}{f_T} B^3 \tag{11}$$

and that the minimum will occur for that value of gate width which makes

$$\frac{C_{gs}}{1 + \gamma} = C_d + C_w \tag{12}$$

We see that the optimized channel current does not depend on γ, although the proper width for reaching optimization does depend on γ. When $\gamma = 0$, then C_{gs} is set equal to $C_d + C_w$ to achieve the least channel noise. This is the ideal (intrinsic) case. When $\gamma \neq 0$, then $C_{gs}/(1 + \gamma)$ is set equal to $C_d + C_w$. This is the practical (extrinsic) case. In either case, the current is the same once the optimization has been carried out.

5. DISCUSSION

Some idea of the minimum noise which can reasonably be attained with the present technology is given by the solid lines in Fig. 1, which are the predictions of equations (5), (6), (8), and (11) for R = 25 kohm/B^{13} with B in Gb s^{-1}, I_d = 100 nA, $C_d + C_w$ = 0.2 pF, and f_T = 10 or 50 GHz. This assumes that the receivers have been optimized and that 1/f noise can confidently be neglected. We see that the hybrid

sensitivities do indeed fall between these two limits. However, the monolithic circuits, with the exception of the 2 Gb s^{-1} result, do not even seem to be designed to match the hybrid results. The large separation of measured and predicted sensitivities remains unexplained except in the one case for which the FET noise was directly measured[2]. In this case, it was found that 1/f noise explained the difference quite well.

The technology of InP based monolithic receiver integration is just coming to grips with the conflicting requirements imposed by the different materials for the photodetector (thick undoped layers) and the FETs (thin precisely doped layers). The circuits themselves are small scale, typically with one stage of modest gain (usually near 10) followed by one impedance matching stage. The noise properties of the FETs themselves are rarely measured, so it is not known whether 1/f noise is a widespread problem. In any case, the noise properties of InP based FETs have not yet been extensively examined.

This is in great contrast with the hybrid receivers, which employ commercially available FETs with high values of f_T and well controlled low noise properties. These FETs are then often assembled in sophisticated designs such as the cascode circuit[10].

6. CONCLUSION

We have examined the noise of practical wide-band receiver circuits and have discovered that the minimum FET noise, attained by adjusting the gate width of the FET, is unaffected by the presence of parasitic resistances R_s and R_g. These parasitics can therefore NOT reduce the discrepancy between observed and predicted sensitivities of monolithic receiver circuits, provided that these circuits have been properly designed for minimum noise.

Monolithic receiver circuits may not reach the high sensitivities of which they are capable until InP based circuitry can achieve a higher level of overall technical development.

7. APPENDIX: NOISE FOR RECEIVERS WITH EXTRINSIC FETs

The treatment of real (extrinsic) FETs taking parasitics into account has been given in detail by Pucel, Haus and Statz[14]. Fukui[12] has been able to show that the expressions given by Pucel, Haus and Statz[14] can be simplified by using them with the following limit:

$$K_g = P = \Gamma$$

$$K_r = 0 \qquad \text{(A1)}$$

$$K_c = 1$$

In this limit, which we shall call the "Fukui limit", the spot (narrow band) noise properties of actual GaAs FETs are very well described. We are interested in applying the Fukui limit in a wide-band scenario where there is no opportunity to adjust the source impedance for minimum noise figure at one specific frequency as is done in the spot noise case.

We begin with equations (95) of Pucel, Haus and Statz[14], which in the Fukui limit are

$$r_n = R_g + R_s \qquad \text{PHS(95a)}$$

$$g_n = \Gamma\ (\omega C_{gs})^2/g_m \qquad \text{PHS(95b)}$$

$$Z_c = R_T + \frac{1}{j\omega C_{gs}} = R_g + R_s + R_i + \frac{1}{j\omega C_{gs}} \qquad \text{PHS(95c)}$$

However, the standard model of receiver noise[11] uses current generators and admittances arranged in a "π" configuration, whereas this representation uses voltage generators and impedances in a "T" configuration. We therefore transform the above expressions for r_n, g_n and Z_c to expressions for R_n, G_n and $Y_c = G_c + jB_c$. The equations for this transformation and the meaning of these quantities are given in Fig. 3 of Rothe and Dalke[15]. We then have expression (14) of Rothe and Dalke for our total effective noise conductance G_{tot}:

$$G_{tot} = G_s + G_n + R_n\ \{(G_s + G_c)^2 + (B_s + B_c)^2\} \qquad \text{RD(14)}$$

Here the subscript "s" refers to an external source admittance. The transformation carried out above results in the following values inherited from the Pucel, Haus, Statz[14] treatment:

$$G_n = (R_g + R_s) g_m^2 (f/f_T)^2/[\ ]$$

$$R_n = R_g + R_s + \frac{\Gamma}{g_m}\ \{1 + R_g g_m\ (f/f_T)^2\}$$

$$G_C = \frac{(R_T g_m)^2 (f/f_T)^2}{R_T} \Big/ [\ ] \qquad (A2)$$

$$B_C = g_m (f/f_T)/[\ ]$$

$$[\ ] = [1 + \gamma + (R_T g_m)^2 (f/f_T)^2]$$

$$\gamma = (R_g + R_S) g_m / \Gamma$$

So far, this development has been exact after imposition of the Fukui limit. We now recognize that for typical FETs g_m will be about 0.1 S and R_T will be about 10 ohms, so that $g_m R_T$ and γ are on the order of 1. We further note that the FETs will only be operating below f_T, so that f/f_T will be less than 1. Using these approximations, we find that

$$G_{tot} \approx G_S + (1 + \gamma) \frac{\Gamma}{g_m} \{G_S^2 + (B_S + \frac{\omega C_{gs}}{1 + \gamma})^2\} \qquad (A3)$$

Identifying G_S with $1/R$ (where R is the feedback resistance) and B_S with $\omega(C_d + C_w)$ we find that

$$G_{tot} \approx \frac{1}{R} + (1 + \gamma) \frac{\Gamma}{g_m} \{\frac{1}{R^2} + \omega^2 (C_d + C_w + \frac{C_{gs}}{1 + \gamma})^2\} \qquad (A4)$$

The total wide-band noise is given by integration of $4kTG_{tot}df$ over frequencies between 0 and B. We thus arrive at a final noise of

$$\frac{4kT}{R} B + 4kT (1 + \gamma) \frac{\Gamma}{g_m} 4\pi^2 (C_d + C_w + \frac{C_{gs}}{1 + \gamma})^2 \frac{B^3}{3} \qquad (A5)$$

after neglecting $1/R^2$ in the bracket of (A4). For $\gamma = 0$ this reduces to the standard model (except for shot noise and pulse shape considerations which, according to the detailed development of Smith and Personick[11], would contribute an I_2 to the first term and replace 1/3 with I_3 in the last term). Furthermore, using equation (22) of Rothe and Dalke[15] it is easy to show, after neglect of high order terms in f/f_T, that these equations (A2) give the correct minimum noise figure used by Fukui.

8. ACKNOWLEDGEMENTS

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APPENDIX B

A Method for Low-Frequency Measurement

of Transistor-Noise Power

POWER VERSUS VOLTAGE: TO MATCH OR NOT TO MATCH?

The central theme in noise analysis is the concept of noise figure, that we will introduce later for deriving a method that uses a spectrum analyzer to measure the noise of a field-effect transistor (FET). Noise figure is based on the ideas of available noise power and power gain, both involve the idea of a match between two networks. These ideas are most useful at high frequencies (1 GHz and beyond), but tend to be unimportant at lower frequencies where voltages are usually used in place of powers.

As an introduction, consider the example of figure B-1: an ideal amplifier with a voltage source V_s (such as a battery) at its input and a network of some kind (such as a spectrum analyzer) at its output. Since an ideal amplifier has an infinite input impedance and zero output impedance, the addition of a resistor R_i in parallel with the input and a resistor R_o in series with the output will allow us to represent a practical amplifier more closely and give us the opportunity to examine how voltages and powers vary when these resistors take on different values. In addition, we have included a finite source resistance R_s and an input resistance for the network, R_n.

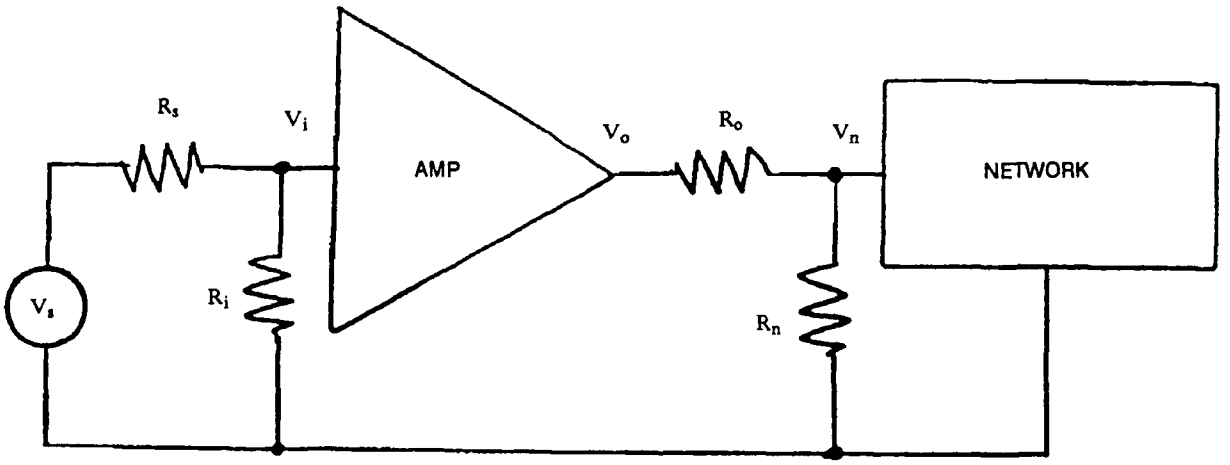

Figure B-1. The simple case of an ideal amplifier fed by a voltage source V_s and examined at its output by a network such as a spectrum analyzer.

We define the following quantities:

$$s_i \equiv \frac{V_i^2}{R_i} \tag{1}$$

$$s_o \equiv \frac{V_o^2}{(R_o + R_n)^2} \tag{2}$$

$$A \equiv \frac{V_o}{V_i} \tag{3}$$

$$g \equiv \frac{s_o}{s_i} \tag{4}$$

Here s_i and s_o are the input and output signal powers, respectively, A is the voltage gain, and g is the power gain.

Regarding the situation where the source resistance R_s stays fixed, we might want to know how the input signal power changes when we use amplifiers with different input resistances. We easily show that the signal power at the amplifier input is

$$s_i = \frac{V_s^2}{4R_s} \bullet \frac{4R_sR_i}{(R_s + R_i)^2} \equiv S_i \bullet M_i \tag{5}$$

where $S_i \equiv V_s^2/4R_s$ is a constant depending only on the source called the *available* input signal power and $M_i \equiv (4R_sR_i)/(R_s + R_i)^2$ is a variable that we shall call the input match. (The input match is connected to the input-reflection coefficient $\Gamma_i \equiv (R_i - R_s)/(R_s + R_i)^2$ by the relation $M_i \equiv 1 - \Gamma_i^2$. When the match is one, the reflection coefficient is zero.) As R_i varies from zero to infinity, M_i rises linearly from zero to a maximum of 1 (when R_i matches R_s), then falls hyperbolically toward zero as R_i becomes larger than R_s. At match, the input power equals the available input power. Off match, the input power is less than the available input power. Stated in more familiar terms, a source delivers a maximum power (called the available power) to a load when the load impedance is matched to the source impedance.

Similar considerations for the signal $S_n \equiv V_n^2/R_n$ at the network input from the amplifier output show that

$$s_n = \frac{V_o^2}{4R_o} \bullet \frac{4R_oR_n}{(R_o + R_n)^2} \equiv S_o \bullet M_o \,. \tag{6}$$

Equation 6 says that the amplifier-output power observed by the network can reach a maximum, equal to $S_o = V_o^2/4R_o$. This maximum, called the *available* output power of the amplifier, depends only on the amplifier. The maximum occurs when the output match $M_o \equiv (4R_oR_n)/(R_o + R_n)^2$ takes on the value 1; that is, when R_n equals R_o. Off match in either direction, the network sees less power.

When dealing with power, a match (or something close to it) is usually sought to gain a significant power transfer from source to load. This requires $R_{load} = R_{source}$

that sets M = 1 and results in a voltage division by a factor of two between source and load. When dealing with voltage the loading of the sensing circuit is usually minimized to maximize the voltage seen by that circuit. This requires $R_{load} >> R_{source}$ that sets M $\approx$ 0 resulting in poor power transfer. However, the source voltage appears almost entirely across the load where it can be observed at nearly full value.

AVAILABLE POWER GAIN

We define the *available* power gain, G, of an amplifier to be the ratio of available powers at output and input:

$$G \equiv \frac{S_o}{S_i} . \tag{7}$$

The available power gain does not depend on the input or output match. The available power gain has nothing to do with the ratio between input and output powers for off-match conditions: in other words, G may not equal g. Available power gains are useful because they can be multiplied together: the denominator for one network equals the numerator for the following network. Using the definitions of available power and noting from figure B-1 that

$$\frac{V_i}{V_s} = \frac{R_i}{(R_i + R_s)} \tag{8}$$

we can derive this alternate expression for the available power gain of an amplifier:

$$G = A^2 M_i \frac{R_i}{4R_o} . \tag{9}$$

Besides providing a useful way to calculate G for a voltage amplifier with known voltage gain, equation 9 explicitly demonstrates that G depends on all of the resistors in figure B-1 except R_n. While we easily see why G depends on R_s and R_o, since these resistances directly determine the available powers in equation 7, it is somewhat difficult to see why G also depends on R_i. The reason is R_i varies, although nothing alters the available power at the input, the available power at the output changes as V_o tracks the changing fraction of the input voltage tapped off the source.

For a perfectly matched input and output, the powers appearing there are equal to the available powers ($s = S$), and the power gain and available power gain are equal ($g = G$). However, as pointed out previously, a voltage amplifier will not be matched: it will have an input impedance larger than the impedance of the source it is observing. In fact, for $R_i >> R_s$,$M_i \approx 4R_s/R_i$, and we have the following approximate expression for the available gain of a voltage amplifier:

$$G \approx A^2 \frac{R_s}{R_o} \tag{10}$$

Note, in this limit the available power gain does become independent of the amplifier input impedance.

We conclude this section with an aside. Many times a voltage such as V_s will be observed with a preamplifier and some instrument that, in the case of the spectrum analyzer, will be displaying the power at its input, s_n. The set-up will be the one shown in figure B-1. We might want to ask "How s_n is related to V_s?" This question can be answered from a power perspective or a voltage perspective. Combining equations 6 and 7 we can write

$$s_n = S_o M_o = S_i G M_o \tag{11}$$

that is useful when considering power. Substituting in the definitions for S_i and M_o and using equation 10 for the available gain in the voltage limit, we have the following equation which is more useful when considering voltage:

$$s_n \approx (AV_s)^2 \frac{R_n}{(R_o + R_n)^2} \tag{12}$$

NOISE FIGURE

From now on, we will use only available power quantities. To be specific, the available noise power will be called "noise" and denoted by N, the available signal power will be called "signal" and denoted by S, and the available power gain will be called "gain" and denoted by G.

In general there will be some noise N_i available at the input to the ideal amplifier pictured in figure B-1, and this noise will be amplified by the gain just like a signal. Besides this input noise, a practical amplifier will also add some of its own noise so that at the output the total noise power will be

$$N_o = N_a + GN_i \tag{13}$$

In this expression N_a is the noise at the amplifier output that is added by noise sources internal to the amplifier.

Equation 13 is deceptively simple: it embraces the notions of noise origin (distinguishing between those internal and external to the amplifier), available noise power, and available gain. Equation 13 uses noise powers added directly; noise voltages, had they been used, would have been added in quadrature.

The noise figure F of an amplifier has been defined by Friis (1944) to be the ratio of the signal-to-noise ratio at the amplifier input to the signal-to-noise ratio at the amplifier output:

$$\begin{aligned} F &= \frac{S_i/N_i}{S_o/N_o} \\ &= \frac{S_i/N_i}{GS_i/(N_a + GN_i)} \\ &= \frac{N_a/GN_i}{GN_i} . \end{aligned} \tag{14}$$

The input noise is usually thermal noise in the incremental bandwidth df:

$$N_i = kTdf \tag{15}$$

where T is the temperature of the source, usually 290 K (denoted by T_o). The power spectral density kT_o is 4.00×10^{-21} watts (–174 dBm) per hertz of bandwidth. The IRE adopted 290 K as the source temperature for determining noise figure, giving the following IRE definition of noise figure:

$$F = \frac{N_a + GkT_odf}{GkT_odf} . \tag{16}$$

Friis (1944) shows that an amplifier with gain G_1 and noise figure F_1 followed by a second amplifier with gain G_2 and noise figure F_2 is equivalent to a single amplifier with gain $G_{12} = G_1G_2$ and noise figure F_{12} where

$$F_{12} = F_1 + \frac{F_2 - 1}{G_1} . \tag{17}$$

Hence,

$$N_{o2} = F_{12}G_{12}N_i = F_{12}G_1G_2N_i \tag{18}$$

gives the noise at the output of the second amplifier. N_1, the noise at the input of the first amplifier, is generally given by equation 15.

In the FET Amplifier section the first amplifier will be a single FET and the second amplifier will be a preamplifier.

THE FET AMPLIFIER

To make use of equation 17, we need to regard the FET and its load resistor shown in figure B-2 in terms of the amplifier shown in figure B-3. What are F and G

for the FET amplifier in figure B-3? (Figures and equations appearing in the main body of this report will be preceded by the letter "M.") Using the equivalent circuit of figure M3 we have an output voltage of $g_m V_{gs} R_d$ when the input voltage is V_{gs}. Hence the voltage gain A is $V_o/V_i = g_m R_d$. The output impedance R_o is R_d, the parallel combination of the actual load resistor R_L and the dynamic FET output resistance r_o. The input impedance for a FET is very high since it is essentially determined by the dynamic resistance associated small leakage currents. Hence equation 10 will be a good approximation to the available power gain of the FET regarded as an amplifier, and substituting for the voltage gain we have

$$G_1 \approx A^2 \frac{R_s}{R_o} = (g_m R_d)^2 \frac{R_s}{R_d} = g_m^2 R_s R_d . \qquad (19)$$

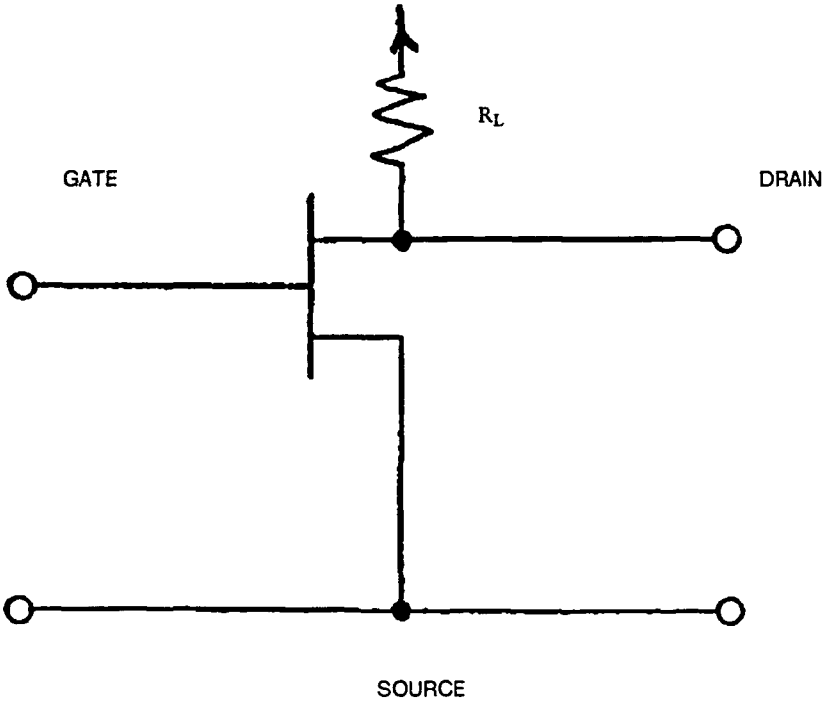

Figure B-2. Discrete FET and load resistor R_L in a common source configuration.

R_s is absent from figure B-3 but would be present in an actual practical circuit in the form of a resistor through which bias would be applied to the gate.

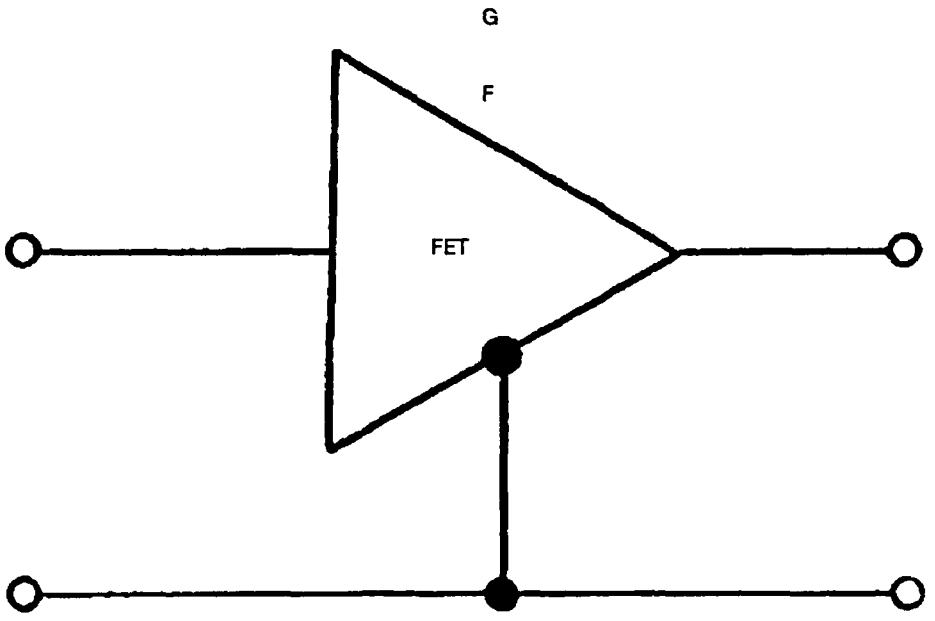

Figure B-3. Two port amplifier with gain G and noise figure F.

The noise added by the FET is represented in figure M3 by the current generator i_n . The power available from this generator at the amplifier output is

$$N_a = \frac{< i_n^2 > R_D}{4} = kTg_m R_d \gamma \, df \tag{20}$$

after making use of M(6). Substituting equation 20 for N_a into the last of equations 14 and using equation 19 for $G \equiv G_1$ and equation 15 for N_i we arrive at the following expression for the noise figure of the FET amplifier:

$$F_1 = 1 + \frac{\gamma}{g_m R_s} . \tag{21}$$

THE RATIO METHOD

The FET noise is generally too small to be seen by the spectrum analyzer alone, so a preamplifier must be placed between the FET and the spectrum analyzer to amplify the FET noise above the noise of the analyzer. Figure B-4 shows the set-up, where each network has its own gain and noise figure. The matching networks are explicitly shown in figure B-4 although they will not enter into any of the formula because

available quantities are being employed. In figure B-4 the noise available at the input of the spectrum analyzer is denoted by N_{o2} and is given analytically by equation 18. Substituting equation 17 into equation 18 we get the following expression for N_{o2}:

$$N_{o2} = F_1 G_1 G_2 N_1 + (F_2 - 1) G_2 N_i \,. \tag{22}$$

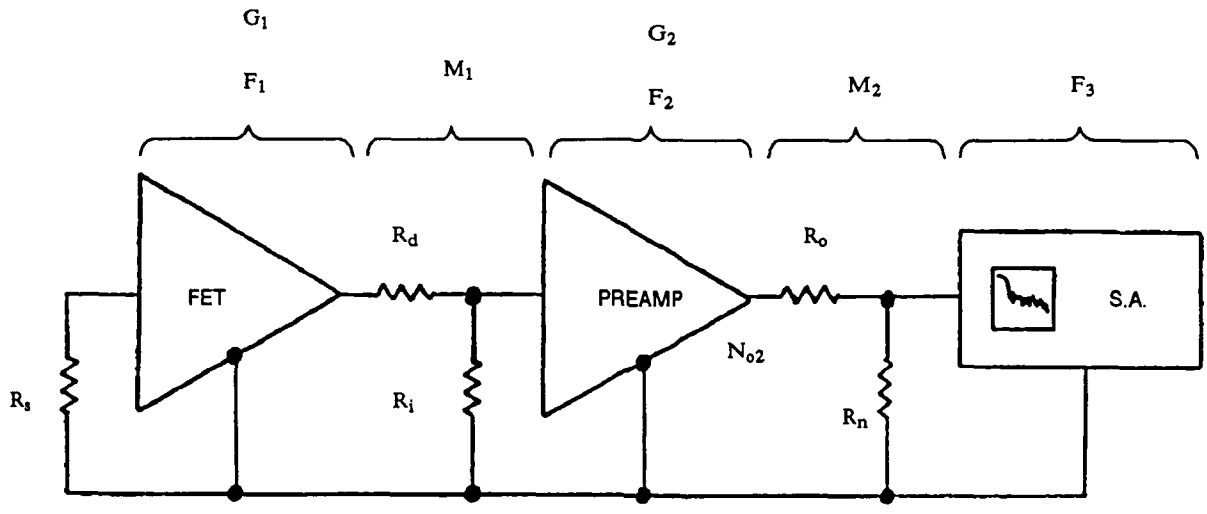

Figure B-4. Set-up for measuring the noise of a FET. F and G are the noise figure and gain, respectively, of each network, and M is the match between each of the networks.

We want to be able to measure F_1 to determine γ through equation 21. We still need to know F_2 and G_2. We can get F_2 from the preamplifier manual or, better yet, from a direct measurement. We can eliminate G_2 by the following ratio technique. Remove the FET and replace it with a resistor equal to R_d. We will then have the set-up of figure B-5 and the available noise power will be

$$N'_{o2} = F_2 G_2 N_i \,. \tag{23}$$

(Note, F_2 and G_2 are identical in equations 22 and 23 only when the input impedance to the preamplifier is the same in figures B-3 and B-4.)

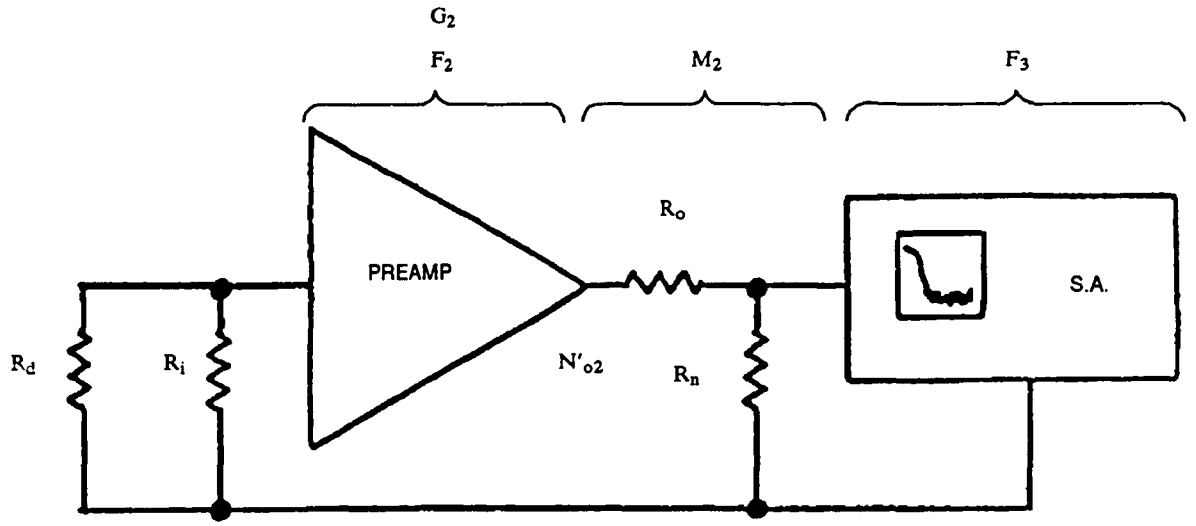

Figure B-5. Set-up for measuring the gain of the preamplifier. Since preamplifier gain depends on input impedance, the gain with this set-up will only equal the gain of figure B-4 if the preamplifier input impedances are the same in both cases.

Defining ρ(f) as the frequency dependent ratio of N_{o2} to N'_{o2},

$$\rho \equiv \frac{N_{o2}}{N'_{o2}} = \frac{F_1G_1G_2 + (F_2 - 1)G_2}{F_2G_2} . \tag{24}$$

Canceling terms and solving for F_1 gives

$$F_1 = \frac{F_2[\rho(f) - 1] + 1}{G_1} = 1 + \frac{\gamma}{g_mR_s} . \tag{25}$$

(Note, F_2 and G_2 are identical in equations 22 and 23 only when the input impedance to the preamplifier is the same in figures B-3 and B-4.)

Solving for γ and using equation 19 for G_1, we finally arrive at the desired relation between γ and ρ:

$$\gamma = \frac{F_2[\rho(f) - 1] + 1}{g_mR_d} - g_mR_s . \tag{26}$$

For our FET, typical values for the quantities appearing in equation 26 are

$$g_m \approx 10\ mS,$$

$$R_d \approx 100\ \Omega$$

$$R_s \approx 50\ \Omega$$

$$F_2 \geq 10,$$

$$\rho(f) \geq 10.$$

which give

$$g_m R_d \approx 1,$$

$$g_m R_s \approx 1/2,$$

and $$G_1 \approx 1/2\ .$$

Therefore, to an accuracy of a few percent

$$\gamma(f) \equiv \Gamma + \frac{f_c}{f} \approx \frac{F_2\ \rho(f)}{g_m R_d}. \qquad (27)$$

The derivation of equation 27 has been the purpose of this appendix.

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The sensitivity of an optoelectronic receiver is determined by its electrical noise. We found that integrated optical receivers made in the past decade are much noisier than hybrid receivers. When the accepted receiver model of Smith and Personick was examined for the cause of this discrepancy, we quickly discovered that the model was missing an important noise source. Is this source, 1/f noise, neglected by Smith and Personick?

1/f noise does exist in indium-phosphide junction field-effect transistors as they are made in our laboratories. The noise corners are within a factor of two of 50 MHz. Since our transistors are probably representative of the indium-phosphide technology as a whole, this means that indium-phosphide-based receivers operating below about 100 MHz will display extra 1/f noise. Circuits operating above about 1 GHz will still have the 1/f noise, but its contribution will be negligible.

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